ERT 5.03.02.2

16 Channel Constant Fraction Discriminator Module

(Data sheet)

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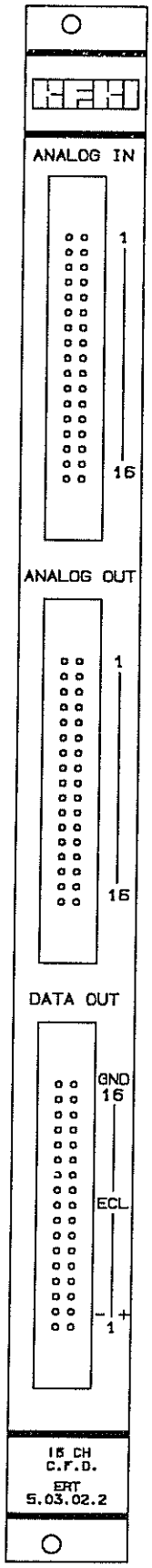


SPECIFICATION

of ERT 5.03.02.2 Type, 16 Channel CFD Module

- Single width VME module
- 16 independent channel
- fraction: 0.3
- dynamic range (analog input: 50Ω): -100mV to - 5V (limited at: -8V)
- DC coupling
- starting threshold settled for each channel separately by VME instructions in the range of: -50mV to -1.0V[1]
- internal CF delay 3-10nsec, settled in 1nsec steps by jumpers (each channel)
- anti-walk discriminator level settled for each channel separately by VME instruction to find walk-minimum at a given signal-form[1]
- Resolution (FWHM): ≤ 25psec, (-0.5V to -5V)
  ≤ 50psec, (-0.1V to -0.5V)
- walk max.: +/-100psec (-100mV to -5V)
  typical: +/-75psec (-100mV to -5V)
- crosstalk[2]: +/-30psec (SM: -1V, SN: -1V)
  +/-100psec (SM: -0.5V, SN: -5V)
- dead time: 20 to 150nsec[3]
- output signal (logical): symmetrical ECL with internal delay: 0 to 100nsec[3]
- analog output signal[4]
  from internal splitter (1/2) and
  with internal delay: 0 to 100nsec[3]
- power requirements: +12V (0.12A), +5V (0.8A)
  -12V (0.20A), -5.2V (3.9A)[5]

Remarks

1 The settled values by VME instructions will be stored in a Non-volatile SRAM while the module is switched off

2 SM: measured signal,
SN: signal on neighbouring channel

3 It should be defined at ordering the module

4 It should be terminated with 50Ω

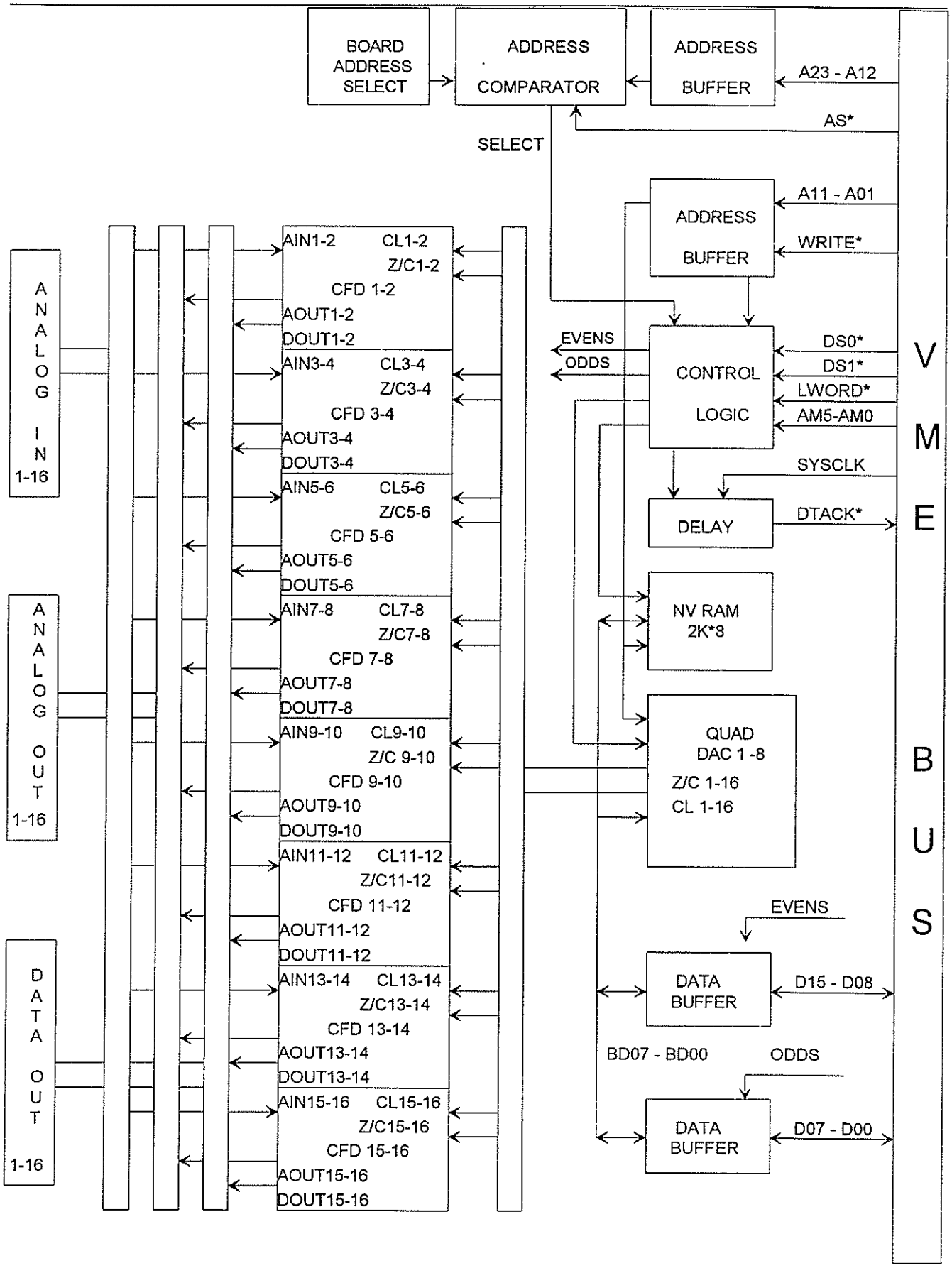
5 Special VME crate required with forced air cooling, equipped also with high current -5.2V power module for ECL circuits

Addresses:

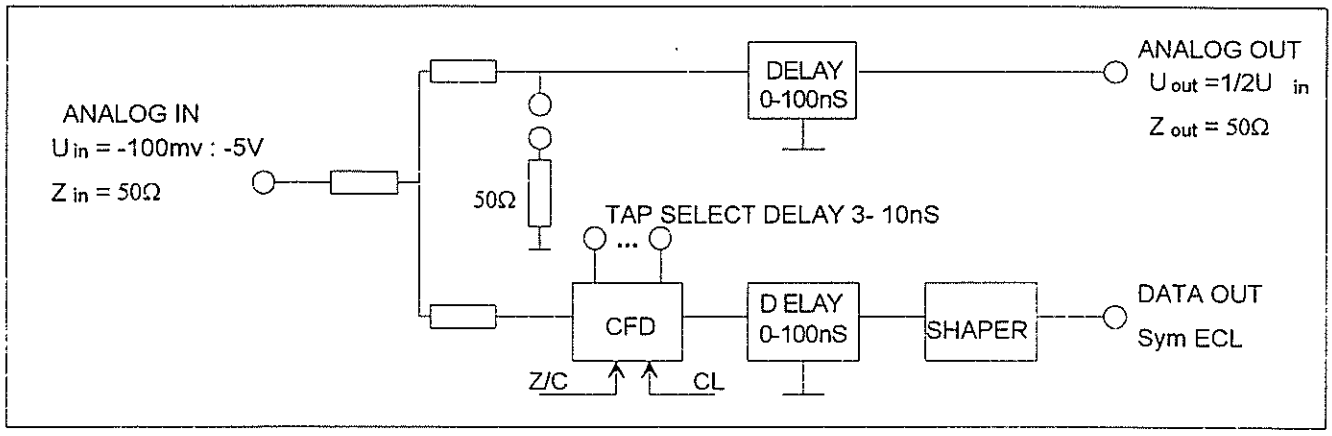
Board base address can be selected with jumper: A23 - A12
Using AM codes: 39h - Standard Non_Privileged Data Access
3Dh - Standard Supervisory Data Access
Non-volatile RAM size: 2k*8 bit, can be spliced into 64*32 byte blocks.
Each block contains 16 byte CL (threshold level) and 16 byte Z/C (anti-walk discr. level) values. The block offset is [(n-1)*20h], where n=block number.
Each data will be loaded parallel into the DAC buffer and the RAM.

Commands:

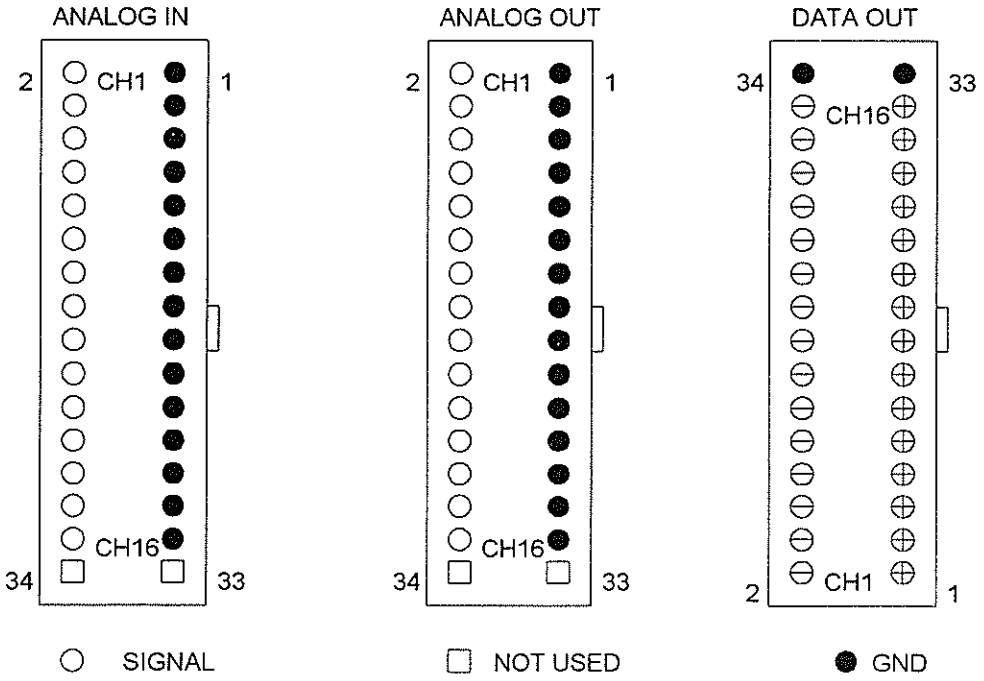
Write CL for cfd 1. channel: board base address+block offset+0h
Write Z/C for cfd 1. channel: board base address+block offset+1h
Write CL for cfd 2. channel: board base address+block offset+2h
Write Z/C for cfd 2. channel: board base address+block offset+3h
Write CL for cfd 3. channel: board base address+block offset+4h
Write Z/C for cfd 3. channel: board base address+block offset+5h
Write CL for cfd 4. channel: board base address+block offset+6h
Write Z/C for cfd 4. channel: board base address+block offset+7h
Write CL for cfd 5. channel: board base address+block offset+8h
Write Z/C for cfd 5. channel: board base address+block offset+9h
Write CL for cfd 6. channel: board base address+block offset+0ah
Write Z/C for cfd 6. channel: board base address+block offset+0bh
Write CL for cfd 7. channel: board base address+blockoffset+0ch
Write Z/C for cfd 7. channel: board base address+block offset+0dh
Write CL for cfd 8. channel: board base address+block offset+0eh
Write Z/C for cfd 8. channel: board base address+block offset+0fh
Write CL for cfd 9. channel: board base address+block offset+10h
Write Z/C for cfd 9. channel: board base address+block offset+11h
Write CL for cfd 10. channel: board base address+block offset+12h
Write Z/C for cfd 10. channel: board base address+block offset+13h
Write CL for cfd 11. channel: board base address+block offset+14h
Write Z/C for cfd 11. channel: board base address+block offset+15h
Write CL for cfd 12. channel: board base address+block offset+16h
Write Z/C for cfd 12. channel: board base address+block offset+17h
Write CL for cfd 13. channel: board base address+block offset+18h
Write Z/C for cfd 13. channel: board base address+block offset+19h
Write CL for cfd 14. channel: board base address+block offset+1ah
Write Z/C for cfd 14. channel: board base address+block offset+1bh
Write CL for cfd 15. channel: board base address+block offset+1ch
Write Z/C for cfd 15. channel: board base address+block offset+1dh
Write CL for cfd 16. channel: board base address+block offset+1eh
Write Z/C for cfd 16. channel: board base address+block offset+1fh
Store RAM data into EEPROM: board base address+800h+write
Restore RAM data from EEPROM: board base address+800h+read
RAM read: board base address+[0 -7ffh]+read



BLOCK DIAGRAM OF THE ERT 5.03.02.2 CFD MODULE



ONE OF THE 16 CHANNELS
BLOCK DIAGRAM



LINE ORDER OF THE CONNECTORS
FRONT PANEL VIEW

Further information:

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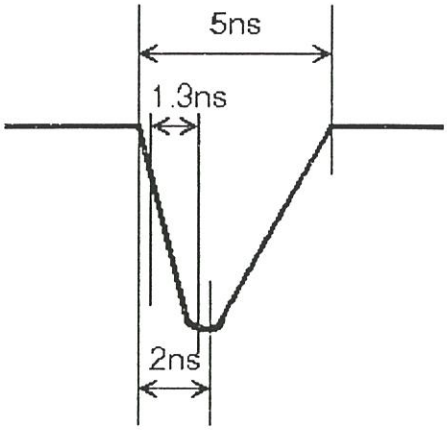
Appendix A

Typical CL and Z/C values at measured pulse:



pulse polarity: negativ
rise time : ~1.3 nS
peak time : 2 nS
total width : 5 nS
optimal tap select delay (0.8-1.2) x rise time.
[~2 ns]

Serial number: 97003

Dead time : ~~50ns~~ 20ns
Analog delay : 0ns
CFD delay : 0ns

Threshold level CL: -150mV
Corresponds at CL DAC output: -350mV

CH1	CL1 DAC	: -350mV
CH2	CL2 DAC	: -350mV
CH3	CL3 DAC	: -350mV
CH4	CL4 DAC	: -350mV
CH5	CL5 DAC	: -350mV
CH6	CL6 DAC	: -350mV
CH7	CL7 DAC	: -350mV
CH8	CL8 DAC	: -350mV
CH9	CL9 DAC	: -350mV
CH10	CL10 DAC	: -350mV
CH11	CL11 DAC	: -350mV
CH12	CL12 DAC	: -350mV
CH13	CL13 DAC	: -350mV
CH14	CL14 DAC	: -350mV
CH15	CL15 DAC	: -350mV
CH16	CL16 DAC	: -350mV

minimal walk for the measured pulse at :

Z/C1	: 400. mV
Z/C2	: 350. mV
Z/C3	: 420. mV
Z/C4	: 400. mV
Z/C5	: 450. mV
Z/C6	: 350. mV
Z/C7	: 350. mV
Z/C8	: 400. mV
Z/C9	: 400. mV
Z/C10	: 350. mV
Z/C11	: 450. mV
Z/C12	: 300. mV
Z/C13	: 400. mV
Z/C14	: 400. mV
Z/C15	: 500. mV
Z/C16	: 400 mV

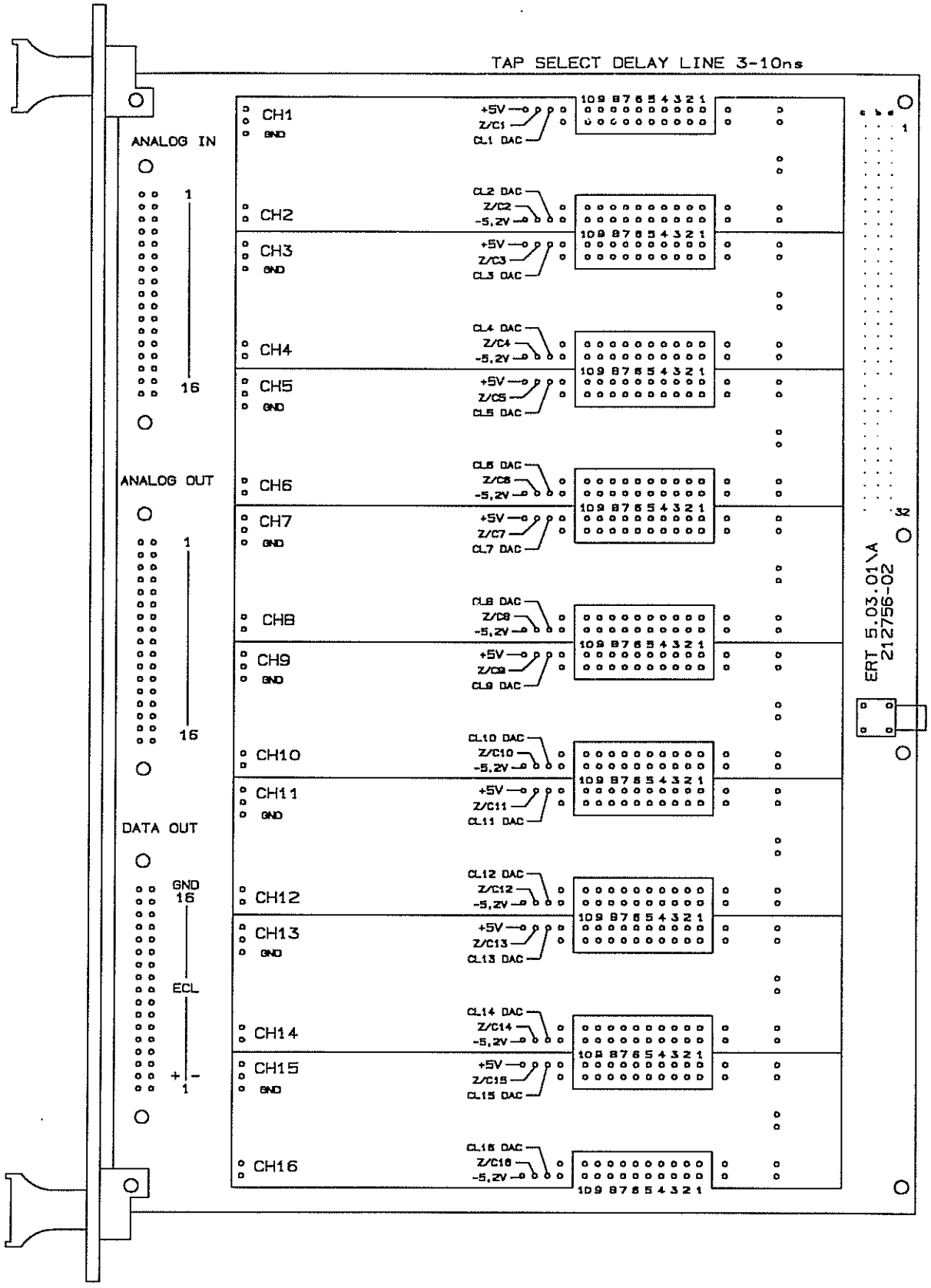
These values were stored into the EEPROM , at switch on will be restored into the RAM automatically. These datas must be transfered into the DAC's buffers.

DAC code table:

DAC data input	Analog output
1 1 1 1 1 1 1 1	+(Vref x (127/128))V
1 0 0 0 0 0 0 1	+(Vref x (1/128))V
1 0 0 0 0 0 0 0	0V
0 1 1 1 1 1 1 1	-(Vref x (1/128))V
0 0 0 0 0 0 0 1	-(Vref x (127/128))V
0 0 0 0 0 0 0 0	-(Vref x (128/128))V

Vref=+2.5V

Appendix B


TAP SELECT DELAY LINE 3-10ns
ANALOG IN
1
16
ANALOG OUT
1
16
DATA OUT
GND
16
ECL
+
-
1
CH1
CH2
CH3
CH4
CH5
CH6
CH7
CH8
CH9
CH10
CH11
CH12
CH13
CH14
CH15
CH16
GND
+5V
-5,2V
Z/C1
Z/C2
Z/C3
Z/C4
Z/C5
Z/C6
Z/C7
Z/C8
Z/C9
Z/C10
Z/C11
Z/C12
Z/C13
Z/C14
Z/C15
Z/C16
CL1 DAC
CL2 DAC
CL3 DAC
CL4 DAC
CL5 DAC
CL6 DAC
CL7 DAC
CL8 DAC
CL9 DAC
CL10 DAC
CL11 DAC
CL12 DAC
CL13 DAC
CL14 DAC
CL15 DAC
CL16 DAC
10 9 8 7 6 5 4 3 2 1
1
32
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